6E1554

Total No. of Questions : 22 Total No. of Pages : 04

Roll No. : .....

6E1554

B.Tech. VI-Sem. (Back) Exam. June - 2024

COMPUTER SCIENCE AND ENGG.

6CS4-04 Computer Architecture and Organization

CS, IT

Time : 3 Hours **Maximum Marks : 120**

Instructions to Candidates :

Attempt all ten questions from Part-A, five questions out of seven questions from Part-B and four questions out of five questions from Part-C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in Form No. 205)

1. ..... 2. .....

PART-A **[10×2=20]**

Answer should be given up to 25 words only

All questions are compulsory

1. Explain tri-state buffer. Describe its role in designing a data bus connecting memory and 4 different I/O interfaces.

2. Design a 4-bit combinational circuit decrementer using four full-adder.

3. Categories instruction cycle into phases and show flowchart by showing working in each timing signal.

4. How does parallel processing benefit modern computer systems and what are the key classifications according to Flynn's Taxonomy?

5. Computer RISC and CISC architectures.

6. Design 64 register stacks and write code for PUSH and POP operations.

7. Explain memory hierarchy in computer system.

8. Explain CPU IOP communications.

9. Explain working of shared memory multiprocessor.

10. Describe address sequencing in control unit.

PART-B

[5×8=40]

Analytical/Problem solving questions

Attempt any five questions

1. Represent $(-185.125)_{10}$ to single precision.

2. Compare first and second pass of an assembler through suitable flowcharts.

3. Consider a pipeline having 4 phases with duration 70, 40, 80 and 100ns. Given latch delay is 10ns calculate-

   (a) Pipeline cycle time

   (b) Non-pipelined execution time

   (c) Speed up-ratio

   (d) Pipeline time for 1000 tasks.

4. Apply Booths algorithms to multiply (-37) and (+21), show the steps involved.

5. Compare the different mapping procedures used in cache memory organization. Give suitable example for each.

6. What are the advantages of using interrupt initiated data transfer over the transfer under program contrast without an interrupt.

7 Illustrate the conditional branch logic to provide decision-making capabilities in the control unit, using suitable diagram.

PART-C

[4×15=60]

Descriptive/Analytical/Problem Solving/ questions

Attempt any four questions

1. Explain memory reference instructions, register reference instructions and Input-Output instruction with a suitable example and instruction cycle.

2. Explain associate memory with its hardware organization. Discuss the procedure for reading and writing data in associative memory.

3. What is priority interrupt? Explain Daisy chain interrupt's polling logic using its block diagram.

4. Describe an algorithm for the restoring method of fixed point binary division. Show the contents of registers during the process of division of 10100011 by 1011.

5. Explain various types of hazards in pipeline structure? Explain these types with the help of suitable example.

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